Abstract of the Disclosure:

A front-end compiler 103 carries out a syntax analysis of a description file 102 describing a desired electronic circuit model with a predetermined high level description language, to generate a control data flow graph 104 having a predetermined graph structure. A back-end compiler 105 divides the control data flow graph 104 into threads composed of a set of a plurality of connected nodes and achieving a particular function. The back-end compiler 105 optimizes the divided threads to meet with a predetermined area restriction and a predetermined waiting time restriction, to obtain designation information of the number, the function, the placement and routing of logic cells for the desired electronic circuit model. According to a compiling method of the present invention, it is possible to describe the electronic circuit model with a high level description language familiar to a programmer, and also it is possible to carry out a further accurate cost estimation.